

M3000

MOTOR AND MOTION CONTROLLER DEVELOPER'S KIT

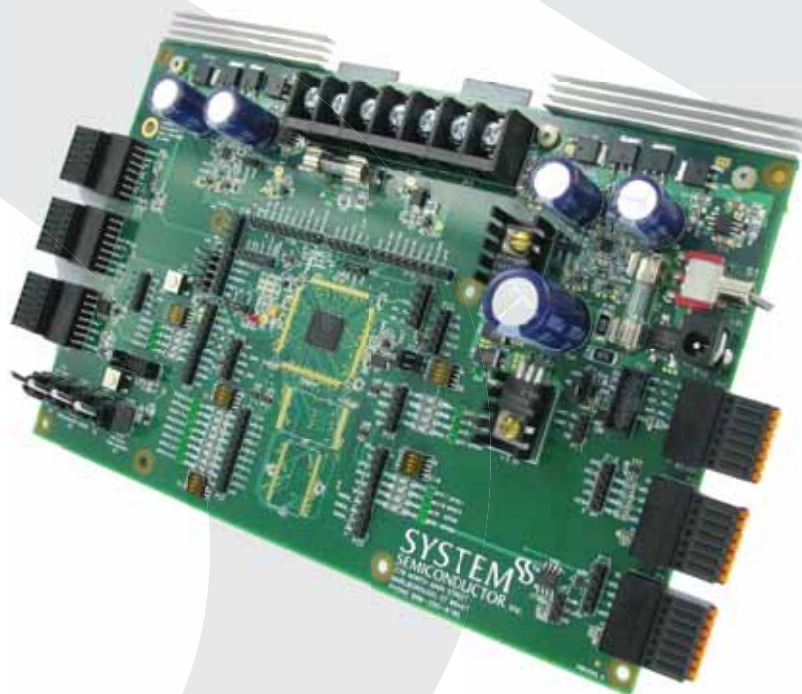


Table of Contents

Section 1: Introduction to the SSI M3000 Developer's Kit	1
M3000	1
IAR Embedded Workbench	1
Kit Features and Contents	2
Section 2: Specifications	3
Electrical Specifications	3
Mechanical Specifications	3
Section 3: Hardware Description	5
Functional Blocks	5
Power	5
Power Cont'd	6
Output Bridges and Stepping Motor	6
Communications	6
Dedicated I/O	6
Encoder	6
General Purpose I/O	6
Block Diagram	7
Section 4: Connectors and Interface	9
Motor and Power	9
P1: Motor/Motor Power Supply	9
P16: Logic Power Supply	10
Communications	10
P14: JTAG-ICE	10
P2 and P8: UART	11
P3: User SPI	12
P4: Master SPI	12
P5: CAN	13
Encoder	13
Dedicated I/O	14
Section 5: Switches and Jumpers	15
Switches	15
Jumpers	16
JP1: RS485 Control	16
JP2: Serial FLASH on Master SPI	16
JP3: FAULT_IN_N	17
JP4: Bridge Enable/Disable	17
Section 6: Test Points	19
Schematic Sheet 1	19
P9: CAN Signals	19
P10: User SPI Test Points	19
P11: UART Test Points	20
P12: Encoder Test Points	20
Schematic Sheet 2	20
P15: Master SPI Test Points	20
Schematic Sheet 3	20
P17: Phase B Current Sense	20
P18: Phase A Current Sense	20
P19: Phase A Control and Feedback	21
P20: Phase B Control and Feedback	21
P21: Trip, Capture, Current and Zero Cross	21
Schematic Sheet 4	22
P22: T0 and T1 Clocks, ICP0	22
P23: Bridge Polarity	22
P24: Bridge Signals	22

Schematic Sheet 5	22
P25: General Purpose I/O 12-19.....	22
P26: General Purpose I/O 8-11, Data Memory Control.....	23
P27: General Purpose I/O 0-3, External Interrupts, Reset	23
P28: Step/Direction I/O, PWM Current Reference.....	23
P29: General Purpose I/O 4-7.....	23
P30: Analog, DAC, Op Amp and Fault_N_N.....	24
Section 7: Installing/Configuring IAR Embedded Work Bench.....	25
Installation/Configuration.....	25

List of Figures

Figure 1.1: SS-DB-3000-B Development Board.....	2
Figure 1.2: SS-PS-100-000 12 VDC Supply.....	2
Figure 1.3: SS-CC-100-000 USB to RS-422 Communication Converter.....	2
Figure 1.4: SS-ICE-V3 USB to JTAG Converter.....	2
Figure 2.1: Development Board Mechanical Specifications.....	3
Figure 3.1: Development Board Functional Blocks and Connector Overview	5
Figure 3.2: Development Board Block Diagram	7
Figure 4.1: Development Board Connector Overview	9
Figure 4.2: P1 - 7-Position Screw Terminal, Motor and Motor Power	9
Figure 4.3: P16 - 2.1 mm Power Jack for Logic Supply.....	10
Figure 4.4: P14 - 12-Pin Header for SS-ICE-V3	10
Figure 4.5: P8 - 10-Pin IDC Header for UART	11
Figure 4.6: P2 - 7-Pin Terminal Block for UART	11
Figure 4.7: P3, 7-Pin Terminal for User SPI	12
Figure 4.8: P4 7-Pin Terminal for Master SPI.....	12
Figure 4.9: P5, 7-Pin Terminal for CAN	13
Figure 4.10: P6, 7-Pin Terminal for Encoder	13
Figure 4.11: P7 7-Pin Terminal for Dedicated I/O	14
Figure 5.1: Development Board Switch Locations	15
Figure 5.2: Development Board Jumper Locations	16
Figure 5.3: JP1 Selection Options	16
Figure 5.4: JP2 Selection Options	16
Figure 5.5: JP3 Selection Options	17
Figure 5.6: JP4 Selection Options	17
Figure 6.1: Test Point Pin Header Locations.....	19
Figure 7.1: Create New C Project.....	25
Figure 7.2: Processor Selection	26
Figure 7.3: Stack Values.....	26
Figure 7.4: Allow C-SPY Extra Output File.....	27
Figure 7.5: Extra output file format.....	27
Figure 7.6 JTAG-ICE Setup.....	28

List of Tables

Table 2.1: DC Electrical Specifications.....	3
Table 4.1: P1 Pin Assignment and Description.....	9
Table 4.2: P14 Pin Assignment and Description.....	10
Table 4.3: P8 Pin Assignment and Description	11
Table 4.4: P3 Pin Assignment and Description	11
Table 4.5: P3 Pin Assignment and Description	12
Table 4.6: P4 Pin Assignment and Description	12
Table 4.7: P5 Pin Assignment and Description	13
Table 4.8: P6 Pin Assignment and Description	13
Table 4.9: P7 Pin Assignment and Description	14
Table 5.1: Development Board Switch Assignment and Description	15
Table 6.1: P9 CAN Signal Test Point Assignment and Description	19
Table 6.2: P10 User SPI Test Point Assignment and Description	19
Table 6.3: P11 UART Test Point Assignment and Description	20
Table 6.4: P12 Encoder Test Point Assignment and Description	20
Table 6.5: P15 Master SPI Test Point Assignment and Description	20
Table 6.6: P17 Phase B Current Sense Test Point Assignment and Description	20
Table 6.7: P18 Phase A Current Sense Test Point Assignment and Description	20
Table 6.8: P19 Phase A Current Control Test Point Assignment and Description	21
Table 6.9: P19 Phase B Current Control Test Point Assignment and Description	21
Table 6.10: P21 Trip, Capture, Current and Zero Cross Test Point Assignment and Description	21
Table 6.11: P22 T0 and T1 Clock, ICP0 Test Point Assignment and Description	22
Table 6.12: P23 Bridge Polarity Test Point Assignment and Description	22
Table 6.13: P24 Bridge Signals Test Point Assignment and Description	22
Table 6.14: P25 General Purpose I/O 12-19 Test Point Assignment and Description	22
Table 6.15: P26 General Purpose I/O 8-11 Test Point Assignment and Description	23
Table 6.16: P27 General Purpose I/O 0-3 Test Point Assignment and Description	23
Table 6.17: P28 Step/Direction I/O, Test Point Assignment and Description	23
Table 6.18: P29 General Purpose I/O 4-7 Test Point Assignment and Description	23
Table 6.19: P30 Analog, DAC, Op Amp Test Point Assignment and Description	24

SECTION 1

Introduction to the SSI M3000 Developer's Kit

Congratulations on your purchase of the M3000 Developer's Kit. This kit is a complete development system for the Systems Semiconductor, Inc. M3000 Motor and Motion Controller.

The M3000 Development Board is for designers writing embedded firmware into the System Semiconductor, Inc. M3000 Motion Controller. To this effect, the Development Board has I/O and communications hardware already installed. The development board also includes an H-Bridge step motor driver providing 0-4 A peak output.

M3000

The System Semiconductor M3000 Motion Controller is a highly integrated, mixed signal system-on-a-chip. The M3000 combines all the major building blocks necessary to control and position multi-phase step motors while also working as a high-speed general purpose microcontroller incorporating extensive communication, analog and system functions.

Integration of System Semiconductor's patented phase current control circuits enables motor performance to reach new limits of increased speed and smoothness while lowering audible noise and vibration. And with System Semiconductor's advanced acceleration, velocity and position control circuits virtually eliminating corresponding time critical tasks, the CPU is freed to perform other system control functions allowing system throughput rivaling high-end DSP's costing far more.

Incorporation of the M3000's extensive communication and general analog functions provides the user the capability to control a large variety of systems without additional circuits.

By integrating all major system's functions into one system-on-a-chip, performance and reliability are greatly enhanced while cost and time to market are reduced. A large temperature range also makes the M3000 ideal for commercial, industrial and automotive applications.

The M3000 uses an Atmel® AVR® core processor with 8-Bit RISC architecture.

IAR Embedded Workbench

The M3000 Development Board interfaces with IAR Embedded Workbench® to format M3000 applications. IAR Embedded Workbench® serves as the front end for code writing and debugging M3000 applications. IAR Embedded Workbench® features a C/C++ compiler and C-SPY™ debugger, assembler, and project manager.

Included with the development kit is a 30-day fully functional evaluation version of IAR Embedded Workbench®. The evaluation version of IAR Embedded Workbench® is completely free of charge. It runs for 30 days and allows you to try the integrated development environment and evaluate its efficiency and ease of use. The only requirement is that you register with IAR to get a license key.

The system requirements for IAR Embedded Workbench® are:

- A Pentium-based PC with Microsoft® Windows® 2000 (SP4) or XP (SP2)
- Internet Explorer 6 or higher
- At least 256 Mbytes of RAM and 200 Mbytes of free disk space
- Adobe® Reader® to access the product documentation
- USB 1.1 or 2.0

Kit Features and Contents

The M3000 Developer's is a complete package to develop motion system applications using the System Semiconductor, Inc. M3000 Motor and Motion Controller ASIC.

The kit contains:

- Development Board featuring:
 - » SS-M3001-B Motor and Motion Controller
 - » 20 Programmable General Purpose I/O with switches to control input states, LEDs to monitor output states
 - » +12 to +75 VDC, 4 A Peak Output Bridge for Motor Control
 - » JTAG Port for programming and debug
 - » UART for RS-422/485 Communications
 - » 2 SPI Ports (User and Master)
 - » CAN Port
 - » Interface for Single-End Encoder
 - » Step/Direction I/O
 - » Capture/Trip I/O
 - » 10-bit Analog Input
 - » Ease of access to test points of all I/O, Bridge Control and miscellaneous functions such as timers and interrupts
 - » Interfacing through pluggable terminal strips.
- SSI USB to JTAG-ICE Converter Cable
- SSI USB to RS-422/485 Communications Converter
- 12 VDC Power Supply to power the motherboard logic
- 30-Day fully functioning trial of IAR Embedded Workbench for Atmel AVR.
- SSI CD's with Developer's Kit Documentation, M3000 Documentation, Schematics and Cable Drivers.



Figure 1.1: SS-DB-3000-B Development Board



Figure 1.2: SS-PS-100-000 12 VDC Supply



Figure 1.3: SS-CC-100-000 USB to RS-422 Communication Converter



Figure 1.4: SS-ICE-V3 USB to JTAG Converter

SECTION 3

Hardware Description

This section provides detailed information on Development Board jumpers, switches and connections. I/O Port headers and connections including SPI communication interface are shown with reference tables.

The Development Board is populated with an SS-M3001-B Motion Controller chip.

The SS-M3001-B has embedded FLASH, 64 x 16 bits, which has a speed of 10MHz.

Critical jumpers have been hard wired, with switches and movable jumpers to be configured in support of an M3000 project. A JTAG port (P14) is provided for program debugging.

During the case of no application or a corrupt application in the program memory, the internal boot monitor in the M3000 will communicate through the SPI or UART port whichever is detected first. A forced reprogram may also be switch initiated (S6).

Communication types available for use are a UART port interfaced to an RS485 transceiver or a CAN port interfaced to a CAN transceiver and two SPI Ports. The RS485 (JP1) transceiver may be jumper selected to transmit enables always, or to be controlled by the M3000.

Functional Blocks

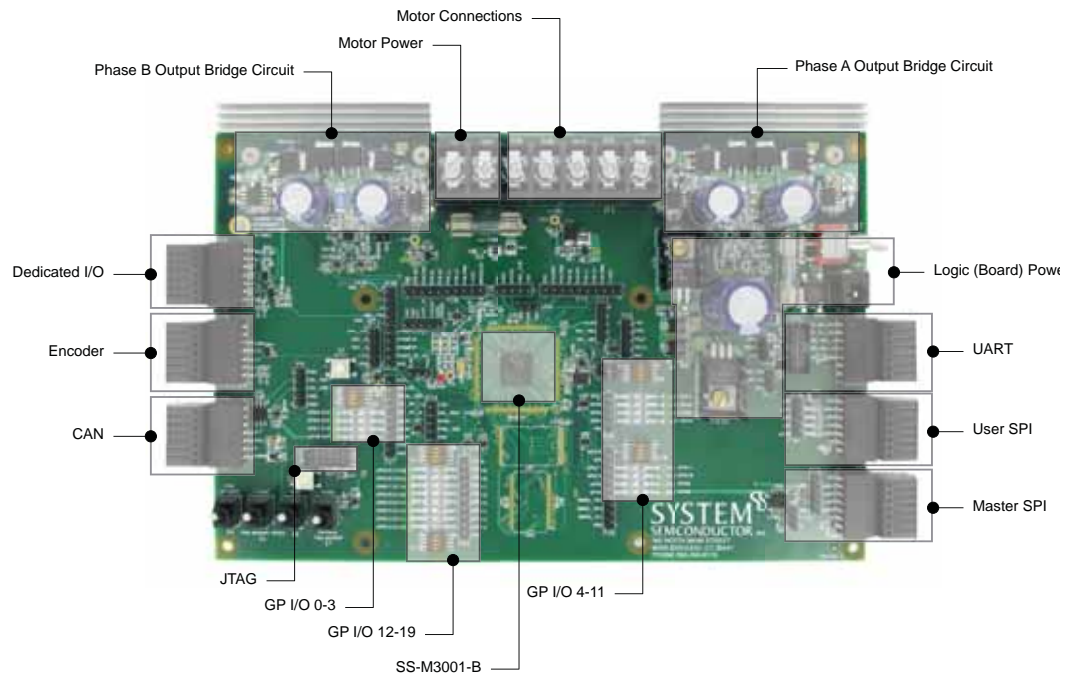


Figure 3.1: Development Board Functional Blocks and Connector Overview

Power

There are two power supplies for the development board:

- Logic Supply (7 to 15 VDC, 225 mA minimum)
- Motor Supply (+12 to +75 VDC)

These power supplies are separated in the interest of safety and efficiency. The only supply voltage needed to develop firmware for the M3000 is the logic supply.

Logic Power

Logic power connects to the 2.1 mm power jack located at connector P16. The range for this supply is 7 to 15 VDC with a minimum current requirement of 225 mA. The center on the jack may be + or - in polarity.

The power supply included with the Developer's Kit is 12 VDC and can supply 1.0 A.

The logic supply is the only supply required to develop firmware for the M3000.

NOTE NOTE: The minimum current requirement for the Logic Supply is 225 mA. If additional circuitry is connected more current may be required.

Power Cont'd**Motor Power**

The development board features a dual H-Bridge with associated current sense signals to provide up to 4 amps of current to a 2-Phase stepping motor.

To power the H-Bridges a +12 to +75 VDC supply is required and will connect to P1 on the Development Board. This power supply only provides power to the H-Bridges and Motor. It does not power any additional circuitry and is not required to develop firmware for the M3000.

If a power supply is needed, supplies designed specifically for use in stepping motor systems may be purchased from Intelligent Motion Systems, Inc. at http://www.imshome.com/pwr_splys.html.

Output Bridges and Stepping Motor

A Stepping Motor may be connected at connector P1 on the development board to test firmware in development. If a stepping motor is required, one may be purchased from Intelligent Motion Systems, Inc. at <http://www.imshome.com/motors.html>.

Communications**JTAG**

The JTAG port is located at connector P14 and is used for programming and debugging using the included USB to JTAG-ICE converter.

UART

The UART may be connected via the 7-pin pluggable terminal at connector P2, or to the 10-pin IDC header at connector P8. If using the included USB to RS-422/485 Communications converter, it will connect to P8.

SPI

There are two SPI Ports, User and Master. Master SPI connects on P4 and User SPI on P3. These would be used if developing applications where SPI is used to configure motion and I/O parameters.

CAN

A CAN port is available at connector P5 and is used in developing applications communicating over a CAN bus using protocols such as CANopen.

Dedicated I/O

The Dedicated I/O connector located at P7 offers accessibility to the dedicated I/O functions of the Development Board. These are:

- Step/Direction
- Trip Out/Capture In
- Analog Input

Encoder

The Development Board includes the ability of interfacing a single-end encoder to connector P6 to aid in developing closed-loop motion applications.

General Purpose I/O

The Development Board features 20 General Purpose I/O Points in 5 groupings of 4 each. These may be exercised as Outputs, with the output state viewed using the onboard LEDs or as inputs using the onboard DIP switches to set the state of the input. As an output, it is best to have the corresponding DIP switch in the open position. The I/O MAY NOT be used to control external devices without additional interface circuitry.

Block Diagram

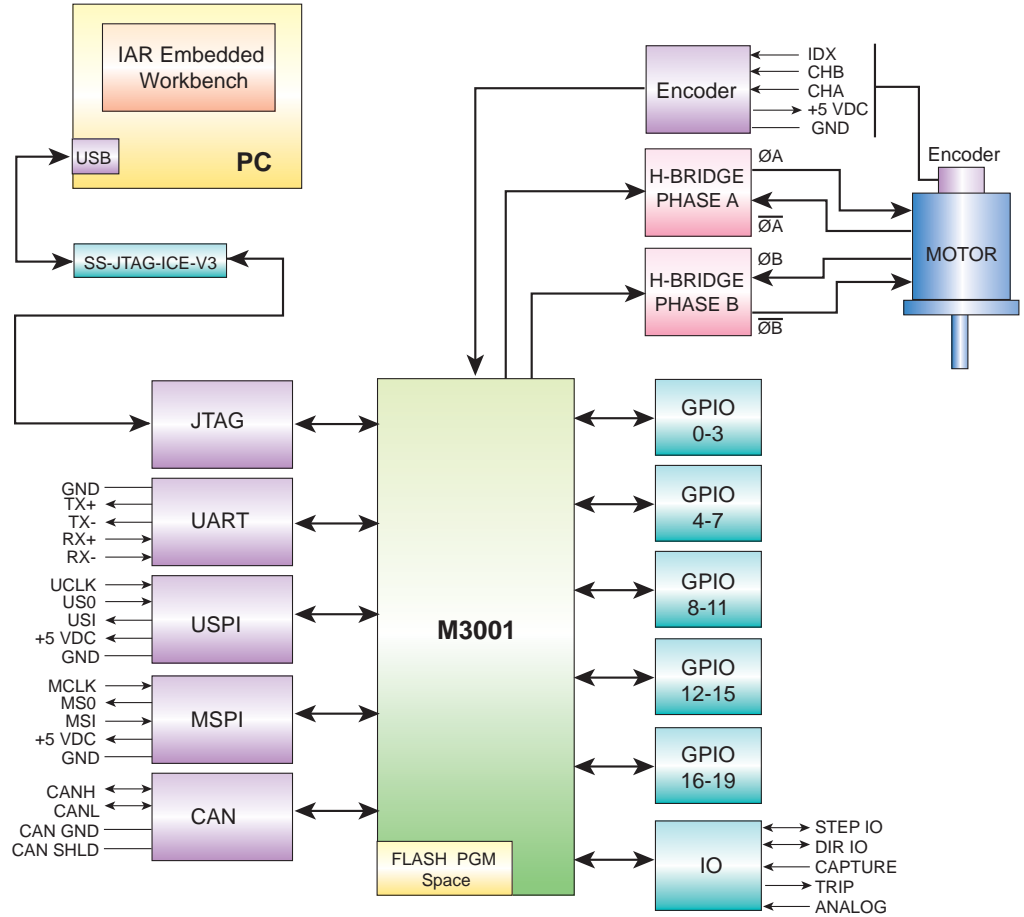


Figure 3.2: Development Board Block Diagram

SECTION 4 Connectors and Interface

This Section will give a detailed look at Connecting and Interfacing to the SSI M3000 Development Board. Connectors will be grouped by function.

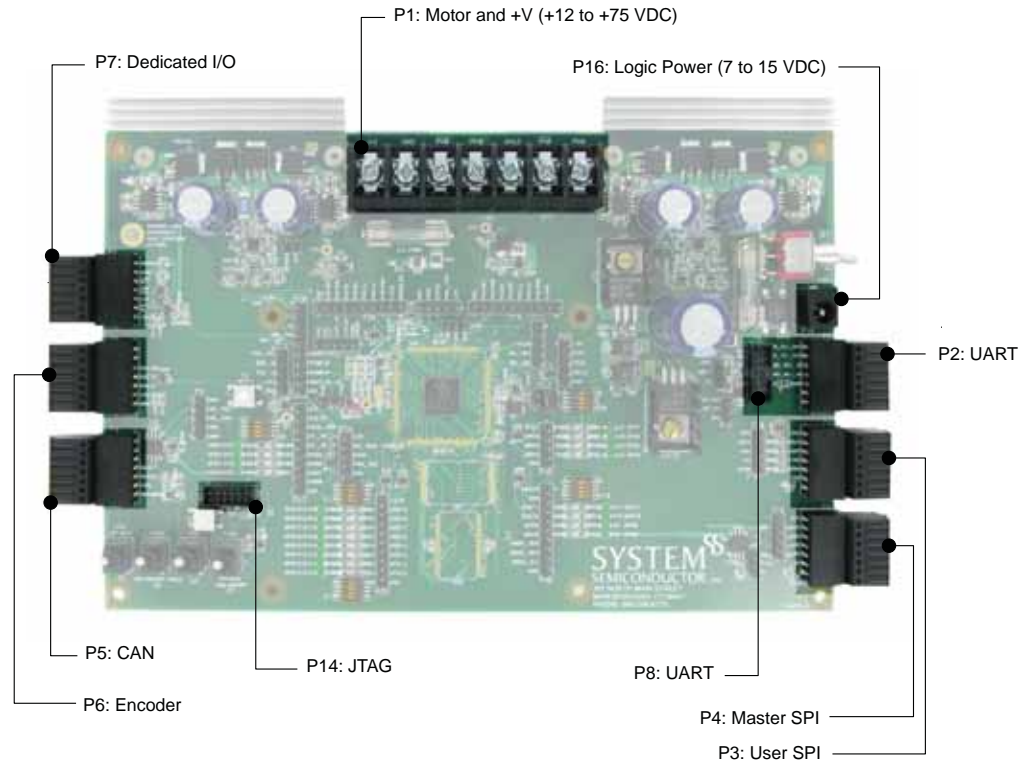


Figure 4.1: Development Board Connector Overview

Motor and Power

P1: Motor/Motor Power Supply

NOTE NOTE: Power and Motor cabling should be shielded twisted pairs. Do not run motor or power cabling parallel with logic or communications wiring to prevent noise coupling.

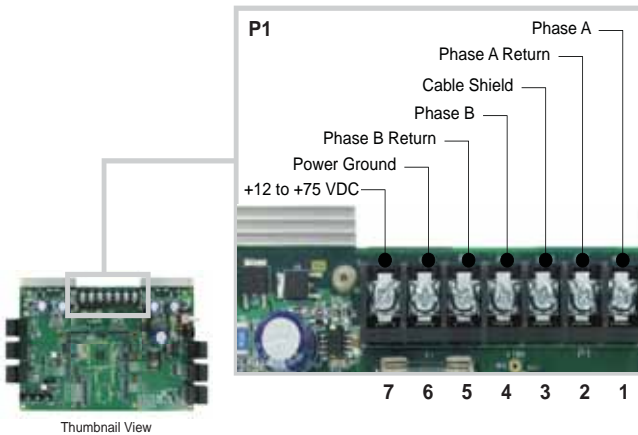


Figure 4.2: P1 - 7-Position Screw Terminal, Motor and Motor Power

Pin Configuration and Description		
Pin #	Function	Description
1	Phase A	Motor Phase A Output, 0.4 to 4 Amps Peak (3A RMS).
2	Phase A	Motor Phase A Return, 0.4 to 4 Amps Peak (3A RMS).
3	SHIELD	Ground Connection used for cable shields only. This terminal MUST NOT be jumpered to Terminal 6 Ground.
4	Phase B	Motor Phase B Output, 0.4 to 4 Amps Peak (3A RMS).
5	Phase B	Motor Phase B Return, 0.4 to 4 Amps Peak (3A RMS).
6	Ground	Motor Power Supply Ground.
7	+V	+12 to +75 VDC power supply input.

Table 4.1: P1 Pin Assignment and Description

P16: Logic Power Supply



NOTE: The 12 VDC Supply included with the Developer's kit is sufficient for all uses of the Development Board, However any 7 to 15 VDC supply with a 2.1 mm jack will work provided it can supply the minimum current of 225 mA. The center pole may be + or -.

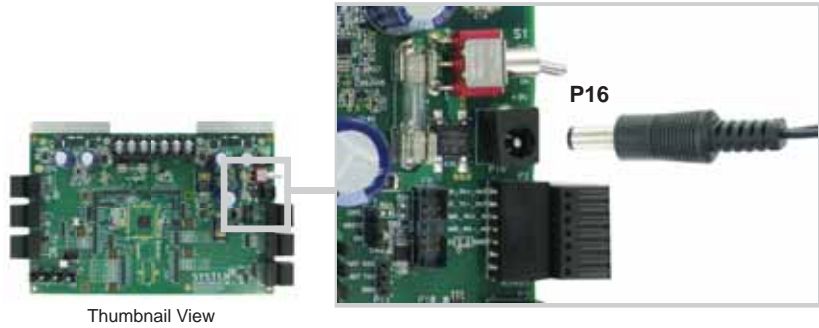


Figure 4.3: P16 - 2.1 mm Power Jack for Logic Supply

Communications

P14: JTAG-ICE

The included USB to JTAG converter for program development/debug plugs directly into the 12-pin header located at connector P14. See Appendices for driver installation instructions.

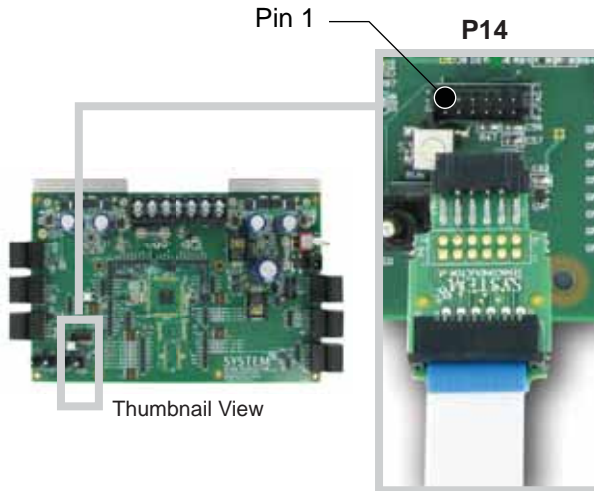


Figure 4.4: P14 - 12-Pin Header for SS-ICE-V3

Pin Configuration and Description		
Pin #	Function	Description
1	IBOOT_N	Internal Boot Input
2	N/C	Not Connected
3	JTAG_TDI	JTAG Emulator Data Input
4	GND	Ground
5	FLASH_SRAM_N	Program Memory Type Input
6	JTAG_RESET	JTAG Reset Input
7	JTAG_TMS	JTAG Emulator Mode Select Input
8	RESET_N	Master Reset Input
9	JTAG_TDO	JTAG Emulator Data Output
10	+5 VDC	+5 VDC
11	JTAG_TCLK	JTAG Emulator Clock Input
12	GND	Ground

Table 4.2: P14 Pin Assignment and Description

P2 and P8: UART

The UART may be interfaced via one of two connectors: P3 (7-Pin Terminal Block) or P8 (10-Pin IDC Header). If using the included USB to RS-422/485 Converter the ribbon cable will plug directly into P8. If using your own converter RS-422/485 may be wired into P3.

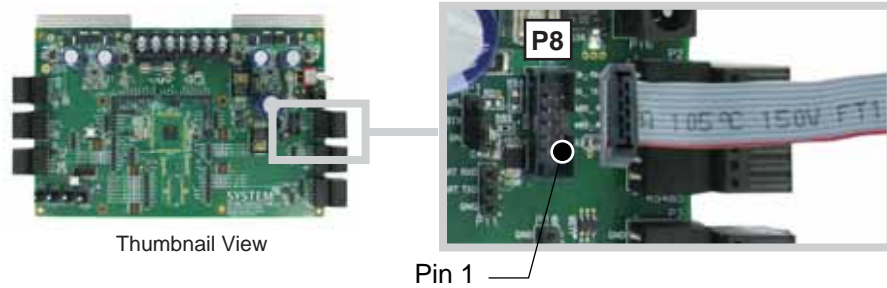


Figure 4.5: P8 - 10-Pin IDC Header for UART

Pin Configuration and Description		
Pin #	Function	Description
1	N/C	Not Connected
2	N/C	Not Connected
3	N/C	Not Connected
4	N/C	Not Connected
5	N/C	Not Connected
6	RX+	Receive Plus - Connects to the TX+ of the RS-422 Host
7	RX-	Receive Minus - Connects to the TX- of the RS-422 Host
8	TX-	Transmit Minus - Connects to the RX- of the RS-422 Host
9	TX+	Transmit Plus - Connects to the RX+ of the RS-422 Host
10	GND	Communications Ground.

Table 4.3: P8 Pin Assignment and Description

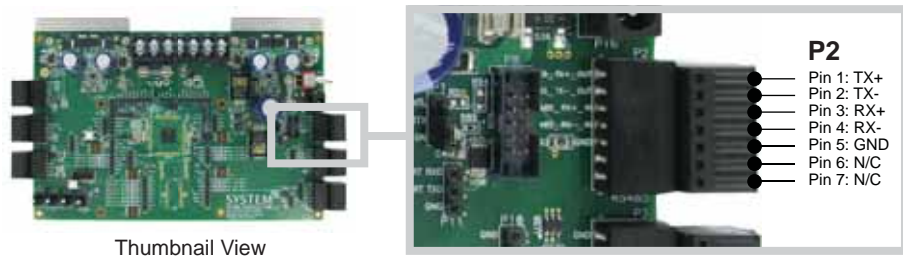


Figure 4.6: P2 - 7-Pin Terminal Block for UART

Pin Configuration and Description		
Pin #	Function	Description
1	TX+	Transmit Plus - Connects to the RX+ of the RS-422 Host
2	TX-	Transmit Minus - Connects to the RX- of the RS-422 Host
3	RX+	Receive Plus - Connects to the TX+ of the RS-422 Host
4	RX-	Receive Minus - Connects to the TX- of the RS-422 Host
5	GND	Communications Ground
6	N/C	Not Connected
7	N/C	Not Connected

Table 4.4: P3 Pin Assignment and Description

P3: User SPI

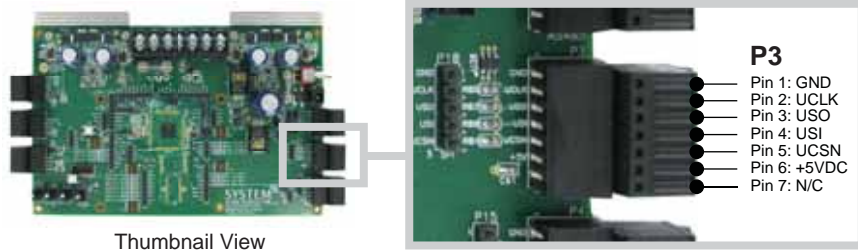


Figure 4.7: P3, 7-Pin Terminal for User SPI

Pin Configuration and Description		
Pin #	Function	Description
1	GND	Communications Ground
2	UCLK	User SPI Clock
3	USO	User SPI Data Out (MISO)
4	USI	User SPI Data In (MOSI)
5	UCSN	User SPI Chip Select Input
6	+5 VDC	+5 VDC used to power converter logic only
7	N/C	Not Connected

Table 4.5: P3 Pin Assignment and Description

P4: Master SPI

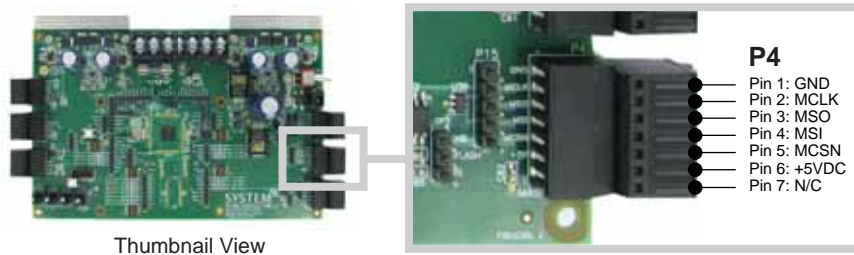


Figure 4.8: P4 7-Pin Terminal for Master SPI

Pin Configuration and Description		
Pin #	Function	Description
1	GND	Communications Ground
2	MCLK	Master SPI Clock
3	MSO	Master SPI Data Out
4	MSI	Master SPI Data In
5	MCSN	Master SPI Chip Select Input
6	+5 VDC	+5 VDC used to power converter logic only
7	N/C	Not Connected

Table 4.6: P4 Pin Assignment and Description

P5: CAN

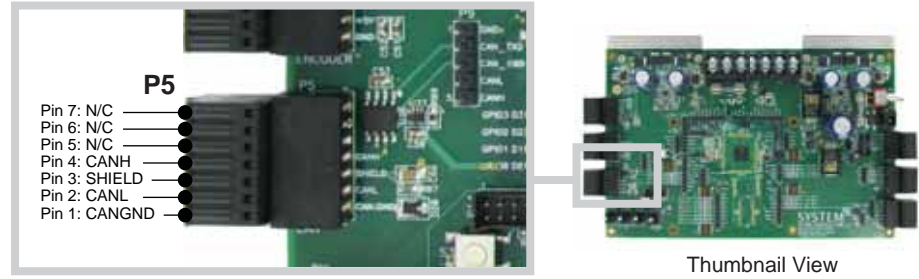


Figure 4.9: P5, 7-Pin Terminal for CAN

Pin Configuration and Description		
Pin #	Function	Description
7	N/C	Not Connected
6	N/C	Not Connected
5	N/C	Not Connected
4	CANH	CAN Bus High
3	Shield	CAN Cable Shield
2	CANL	CAN Bus Low
1	CANGND	CAN Bus Ground

Table 4.7: P5 Pin Assignment and Description

Encoder

The Development Board allows for the development of closed loop motion applications via a single-end encoder connected to the 7-pin pluggable terminal located at P6.

The encoder inputs are quadrature.

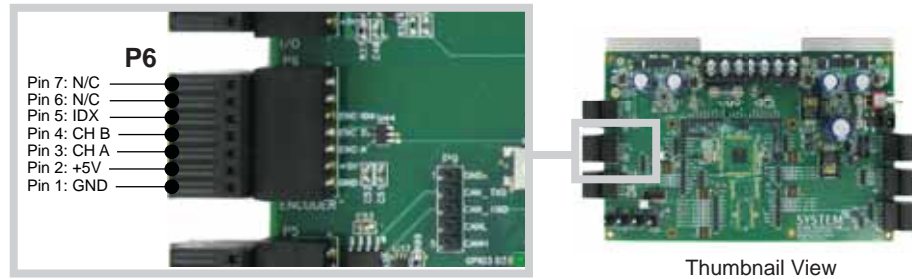


Figure 4.10: P6, 7-Pin Terminal for Encoder

Pin Configuration and Description		
Pin #	Function	Description
7	N/C	Not Connected
6	N/C	Not Connected
5	ENC IDX	Encoder Index Mark
4	ENC CH B	Encoder Channel B
3	ENC CH A	Encoder Channel A
2	+5V	+5 VDC Output. Used to ONLY power an encoder. do not use to power other external devices.
1	GND	Ground

Table 4.8: P6 Pin Assignment and Description

Dedicated I/O

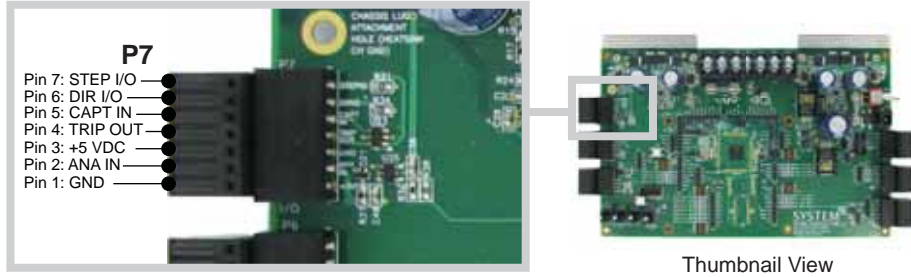


Figure 4.11: P7 7-Pin Terminal for Dedicated I/O

Pin Configuration and Description		
Pin #	Function	Description
7	STEP I/O	Step Clock Input/Output
6	DIR I/O	Direction Input/Output
5	CAPT IN	Capture Input allows for extended event interrupt.
4	TRIP OUT	Trip Output used for netting output from within program control
3	+5 VDC	+5 VDC Output
2	ANA IN	Analog Input configured as a 0 to 5 V, 10 Bit resolution input offering the ability to receive input from various forms of analog sensor.
1	GND	I/O Ground

Table 4.9: P7 Pin Assignment and Description

SECTION 5

Switches and Jumpers

Switches

This section covers the switches and jumpers on the Development Board

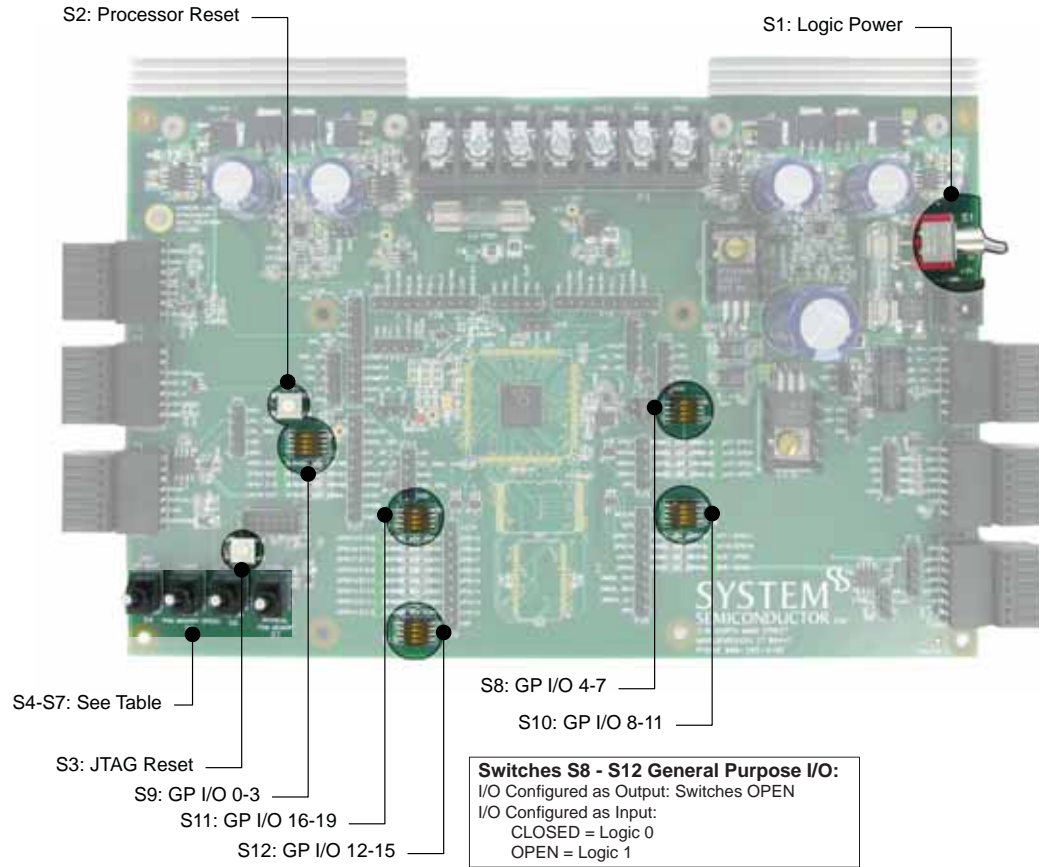


Figure 5.1: Development Board Switch Locations

Switch Configuration		
Switch	Function	Description
S1	Logic Power	Will switch on logic power supply.
S2	Processor Reset	Momentary Switch will reset the M3000 when depressed
S3	JTAG Reset	Momentary Switch will reset the JTAG port when depressed
S4	Internal Boot	Internal BOOT hardware vector upon reset, if populated, this switch should be in the open position.
S5	Program Memory Speed	Set for FLASH, if populated, this switch should be in the open position.
S6	Force Reprogram	Forced reprogram mode (closed), run normal mode (open), if populated, this switch should be in the open position.
S7	Memory Select	SRAM (closed) or FLASH (open), if populated, this switch should be in the open position.
S8 - S12	GPIO	4 Position DIP Switches. If I/O is being used as an Output, the switch associated with the point being used should be open. If I/O is being used as an Input, the switch associated with the point may be used to control the state of the input: Closed = Logic 0 Open = Logic 1

Table 5.1: Development Board Switch Assignment and Description

Jumpers

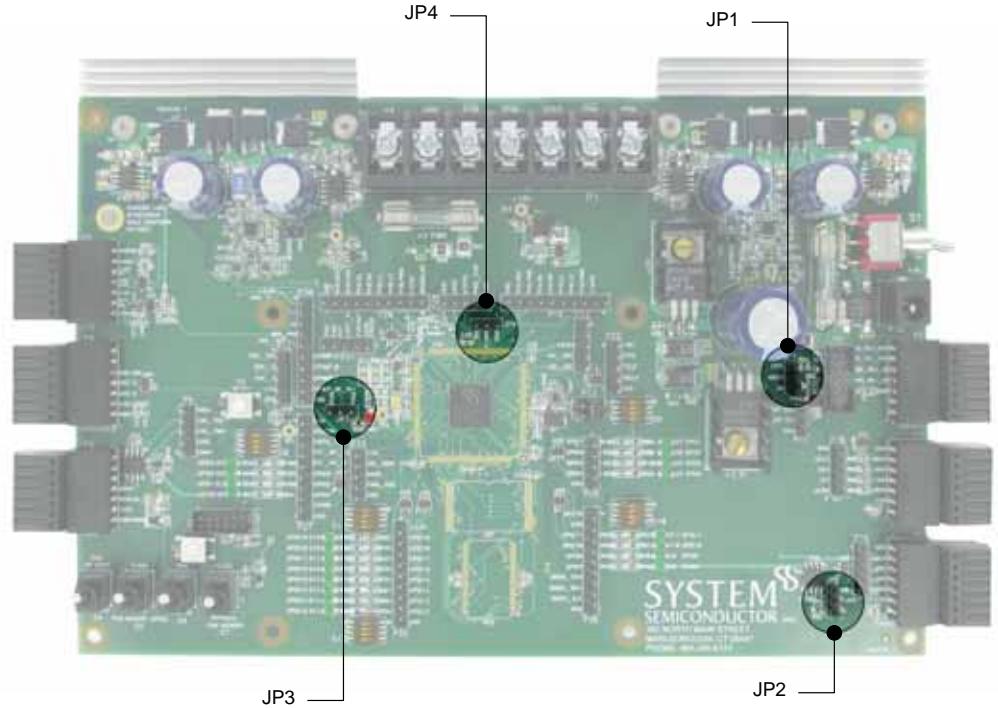


Figure 5.2: Development Board Jumper Locations

JP1: RS485 Control

JP1 determines whether or not the UART is always enabled (default) or controlled by the M3000.



Figure 5.3: JP1 Selection Options

JP2: Serial FLASH on Master SPI

JP2 enables or disables (default) serial FLASH on the Master SPI Port.

NOTE NOTE: JP2 will only be used if the RAM chip is populated on the board and the development board is populated with the 160 QFP package of the M3000.

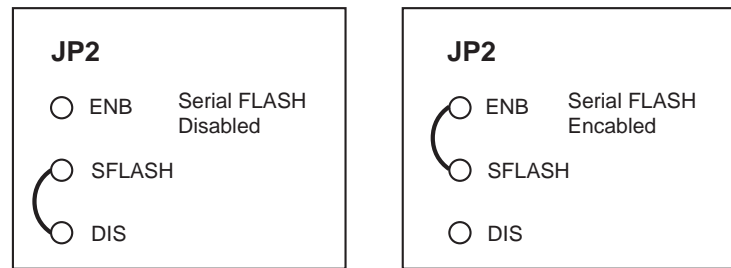


Figure 5.4: JP2 Selection Options

JP3: FAULT_IN_N

JP3 Controls the RUN (default) or FAULT status of the bridge.

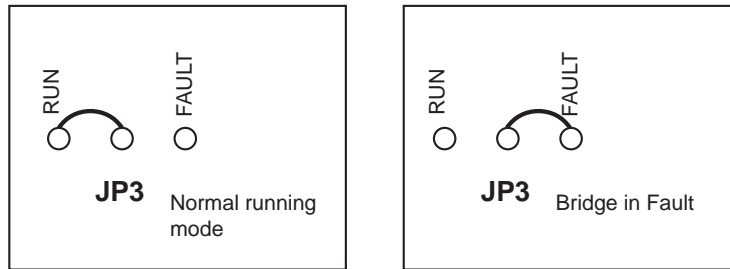


Figure 5.5: JP3 Selection Options

JP4: Bridge Enable/Disable

JP4 Controls the Enabled (default) or Disabled state of the output bridge.

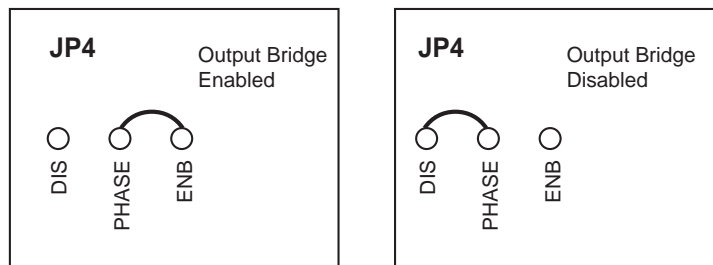


Figure 5.6: JP4 Selection Options

SECTION 6

Test Points



NOTE: Schematics are located on the SSI Developer's Kit CD and are only available with the purchase of the Developer's Kit.

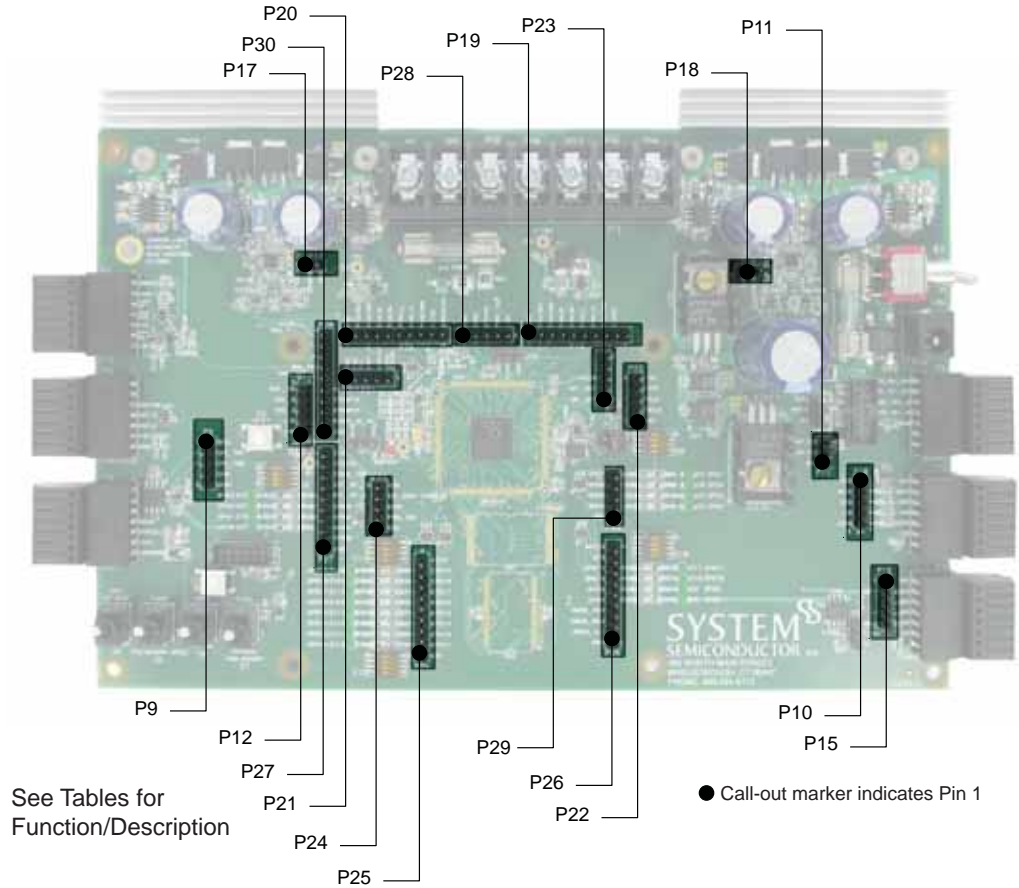


Figure 6.1: Test Point Pin Header Locations

Schematic Sheet 1

P9: CAN Signals

Test Point Configuration and Description		
Pin #	Function	Description
1	GND	Ground
2	CAN_TXD	CAN Transmit Data Output (Transceiver Input)
3	CAN_RXD	CAN Receive Data Output (Transceiver Input)
4	CAN_H	CAN Bus High (Transceiver Output)
5	CAN_L	CAN Bus Low (Transceiver Output)

Table 6.1: P9 CAN Signal Test Point Assignment and Description

P10: User SPI Test Points

Test Point Configuration and Description		
Pin #	Function	Description
1	GND	Ground
2	UCLK	User SPI Clock Output
3	USO	User SPI Serial Output (MISO)
4	USI	User SPI Serial Input (MOSI)
5	UCSN	User SPI Chip Select

Table 6.2: P10 User SPI Test Point Assignment and Description

P11: UART Test Points

Test Point Configuration and Description		
Pin #	Function	Description
1	GND	Ground
2	UART_RXD	UART Receive Data
3	UART_TXD	UART Transmit Data

Table 6.3: P11 UART Test Point Assignment and Description
P12: Encoder Test Points

Test Point Configuration and Description		
Pin #	Function	Description
1	GND	Ground
2	+5 VDC	+ 5 VDC Output
3	ENC_A	Encoder Channel A Input
4	ENC_B	Encoder Channel B Input
5	ENC_IDX	Encoder Index Input

Table 6.4: P12 Encoder Test Point Assignment and Description
Schematic Sheet 2
P15: Master SPI Test Points

Test Point Configuration and Description		
Pin #	Function	Description
1	GND	Ground
2	MCLK	Master SPI Clock Output
3	MSO	Master SPI Serial Output
4	MSI	Master SPI Serial Input
5	MCSN	Master SPI Chip Select

Table 6.5: P15 Master SPI Test Point Assignment and Description
Schematic Sheet 3
P17: Phase B Current Sense

Test Point Configuration and Description		
Pin #	Function	Description
1	GND	Ground
2	SENSEB	Phase B Current Sense

Table 6.6: P17 Phase B Current Sense Test Point Assignment and Description
P18: Phase A Current Sense

Test Point Configuration and Description		
Pin #	Function	Description
1	GND	Ground
2	SENSEA	Phase A Current Sense

Table 6.7: P18 Phase A Current Sense Test Point Assignment and Description

P19: Phase A Control and Feedback

Test Point Configuration and Description		
Pin #	Function	Description
1	GND	Ground
2	PHA_REV	Bridge Control Phase A Reverse Input
3	PHA_FWD	Bridge Control Phase A Forward Input
4	PHA_RL	Bridge Control Phase A Right Low Output
5	PHA_RH	Bridge Control Phase A Right High Output
6	PHA_LL	Bridge Control Phase A Left Low Output
7	PHA_LH	Bridge Control Phase A Left High Output
8	PHA_PWM	Bridge Control Phase A PWM Output
9	V_SIN	DAC Sine Output
10	N/C	Not Connected

Table 6.8: P19 Phase A Current Control and Feedback Test Point Assignment and Description

P20: Phase B Control and Feedback

Test Point Configuration and Description		
Pin #	Function	Description
1	GND	Ground
2	PHB_REV	Bridge Control Phase B Reverse Input
3	PHB_FWD	Bridge Control Phase B Forward Input
4	PHB_RL	Bridge Control Phase B Right Low Output
5	PHB_RH	Bridge Control Phase B Right High Output
6	PHB_LL	Bridge Control Phase B Left Low Output
7	PHB_LH	Bridge Control Phase B Left High Output
8	PHB_PWM	Bridge Control Phase B PWM Output
9	V_COS	DAC Cosine Output
10	BRIDGE.EN	Bridge Enable Output

Table 6.9: P19 Phase B Current Control and Feedback Test Point Assignment and Description

P21: Trip, Capture, Current and Zero Cross

Test Point Configuration and Description		
Pin #	Function	Description
1	GND	Ground
2	TRIP_OUT	Trip Output
3	CAPT_IN	Capture Input
4	CUR_OUT	Current Reference (Reference DAC Output)
5	ZERO_CROSS	Zero Crossing Output

Table 6.10: P21 Trip, Capture, Current and Zero Cross Test Point Assignment and Description

Schematic Sheet 4

P22: T0 and T1 Clocks, ICP0

Test Point Configuration and Description		
Pin #	Function	Description
1	GND	Ground
2	TOCLK	Timer T/C 0 Clock Input
3	T1CLK	Timer T/C 1 Clock Input
4	ICP0	Timer 0 Capture Input
5	+5VDC	+5 VDC Output

Table 6.11: P22 T0 and T1 Clock, ICP0 Test Point Assignment and Description

P23: Bridge Polarity

Test Point Configuration and Description		
Pin #	Function	Description
1	INV_LBC	Invert Low Bridge Control Input
2	INV_HBC	Invert High Bridge Control Input
3	+3.3V	+3.3 V Output
4	N/C	Not Connected
5	N/C	Not Connected

Table 6.12: P23 Bridge Polarity Test Point Assignment and Description

P24: Bridge Signals



NOTE: P23 Signals, with the exception of +5V and GND are N/C, Not Connected

on the version Development Board using the SS-M3001-B 128 BGA

Test Point Configuration and Description		
Pin #	Function	Description
1	GND	Ground
2	PWM_OSC	PWM Oscillator Output
3	MASK	Mask Output
4	SIN_SIGN	Sine Sign Output
5	+5V	+5 VDC Output

Table 6.13: P24 Bridge Signals Test Point Assignment and Description

Schematic Sheet 5

P25: General Purpose I/O 12-19



NOTE: GPIO 8-19 may also be used to connect peripheral devices. See the full

M3000 Product Manual.

Test Point Configuration and Description		
Pin #	Function	Description
1	GND	Ground
2	GPIO12	General Purpose I/O 12/Data Memory Address 0
3	GPIO13	General Purpose I/O 13/Data Memory Address 1
4	GPIO14	General Purpose I/O 14/Data Memory Address 2
5	GPIO15	General Purpose I/O 15/Data Memory Address 3
6	GPIO16	General Purpose I/O 16/Data Memory Address 4
7	GPIO17	General Purpose I/O 17/Data Memory Address 5
8	GPIO18	General Purpose I/O 18/Data Memory Address 6
9	GPIO19	General Purpose I/O 19/Data Memory Address 7
10	3.3V	3.3 VDC Output

Table 6.14: P25 General Purpose I/O 12-19 Test Point Assignment and Description

**P26: General Purpose I/O 8-11,
Data Memory Control**



NOTE: P26 Pin 9,
OCB, is N/C, Not
Connected on the
version Development

Board using the SS-M3001-B 128
BGA

Test Point Configuration and Description		
Pin #	Function	Description
1	GND	Ground
2	DMEM_ALE	Data Memory Address Latch Enable Output
3	DMEM_WEN	Data Memory Address Write Enable Output
4	DMEM_OEN	Data Memory Output Enable Output
5	GPIO8	General Purpose I/O 8/Data Memory Address 8
6	GPIO9	General Purpose I/O 9/Data Memory Address 9
7	GPIO10	General Purpose I/O 10/Data Memory Address 10
8	GPIO11	General Purpose I/O 11/Data Memory Address 11
9	OCB	Timer B Compare Output
10	MHZ20	20 MHz Processor Clock Output

Table 6.15: P26 General Purpose I/O 8-11 Test Point Assignment and Description

**P27: General Purpose I/O 0-3,
External Interrupts, Reset**



NOTE: P27 Pin 10,
OCA, is N/C, Not
Connected on the
version Development

Board using the SS-M3001-B 128
BGA

Test Point Configuration and Description		
Pin #	Function	Description
1	GND	Ground
2	GPIO0	General Purpose I/O 0
3	GPIO1	General Purpose I/O 1
4	GPIO2	General Purpose I/O 2
5	GPIO3	General Purpose I/O 3
6	EXT_INT_0	External Interrupt Input 0 (Programmable Polarity)
7	EXT_INT_1	External Interrupt Input 1 (Programmable Polarity)
8	DMEM_CEN	Data Memory Chip Enable
9	RESETN	Master Reset Input
10	OCA	Timer A Compare Output

Table 6.16: P27 General Purpose I/O 0-3, External Interrupts and, Reset Test Point Assignment and Description

**P28: Step/Direction I/O, PWM
Current Reference**

Test Point Configuration and Description		
Pin #	Function	Description
1	GND	Ground
2	DIRIO	Direction I/O
3	STEPIO	Step Clock I/O
4	PWM_CUR	PWM Current Reference
5	+5V	+5 VDC Output

Table 6.17: P28 Step/Direction I/O, PWM Current Reference Test Point Assignment and Description

P29: General Purpose I/O 4-7

Test Point Configuration and Description		
Pin #	Function	Description
1	GND	Ground
2	GPIO4	General Purpose I/O 4
3	GPIO5	General Purpose I/O 5
4	GPIO6	General Purpose I/O 6
5	GPIO7	General Purpose I/O 7

Table 6.18: P29 General Purpose I/O 4-7 Test Point Assignment and Description

P30: Analog, DAC, Op Amp and Fault_N_N

Test Point Configuration and Description		
Pin #	Function	Description
1	GND	Ground
2	FAULT_N_N	Fault Input
3	OPAMP_P	General Purpose Op Amp Plus Input
4	OPAMP_M	General Purpose Op Amp Minus Input
5	OPAMP_OUT	General Purpose OP Amp Output
6	DAC_OUT	General Purpose DAC Output
7	ANA_PIN	ADC Input or MUX Output
8	ADC_IN	General Purpose ADC Input
9	ANA_IN	Analog Input
10	+3.3V	+3.3 VDC Output

Table 6.19: P30 Analog, DAC, Op Amp and Fault_N_N Test Point Assignment and Description

SECTION 7

Installing/ Configuring IAR Embedded Work Bench

Installation/ Configuration

The M3000 Development Board interfaces with IAR Embedded Workbench® to format M3000 applications. IAR Embedded Workbench® serves as the front end for code writing and debugging M3000 applications. IAR Embedded Workbench® features a C/C++ compiler and C-SPY™ debugger, assembler, and project manager.

Included with the development kit is a 30-day fully functional evaluation version of IAR Embedded Workbench®. The evaluation version of IAR Embedded Workbench® is completely free of charge. It runs for 30 days and allows you to try the integrated development environment and evaluate its efficiency and ease of use. The only requirement is that you register to get a license key.

The system requirements for IAR Embedded Workbench® are:

- A Pentium-based PC with Microsoft® Windows® 2000 (SP4) or XP (SP2)
 - Internet Explorer 6 or higher
 - At least 256 Mbytes of RAM and 200 Mbytes of free disk space
 - Adobe® Reader® to access the product documentation
 - USB 1.1 or USB 2.1
1. Connect and install SSI JTAG-ICE Cable and drivers from the supplied CD, the JTAG drivers may also be downloaded from the SSI web site at <http://www.systemsemi.com>.
 2. Install IAR Embedded Workbench. You will have to register with IAR to receive the free 30-day license key to complete installation.
 3. Open IAR Embedded Workbench.

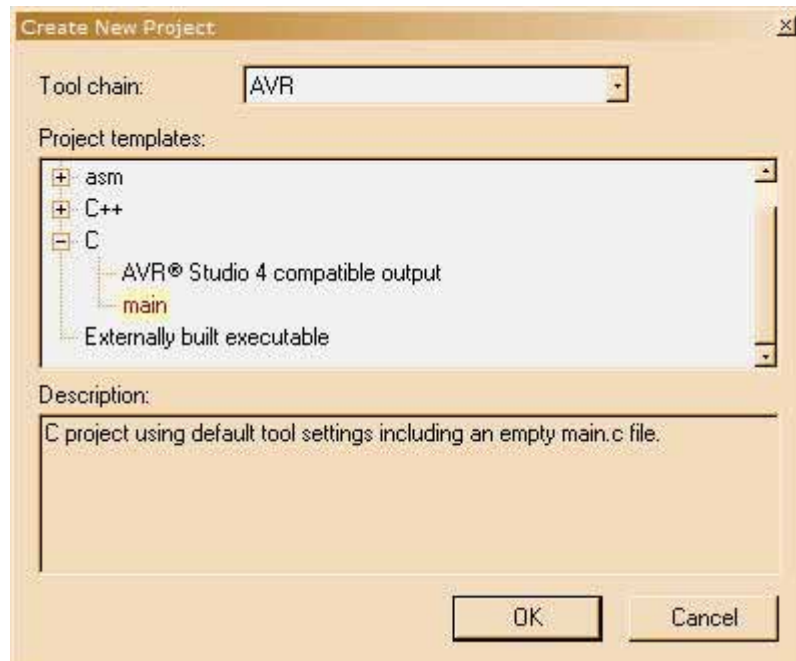


Figure 7.1: Create New C Project

4. Create new Project selecting C > main (Figure 7.1).
5. Save as M3000.ewp
6. Select Project > Add Files. Browse to the SSI Developer's Kit CD folder /samples and select DevBdExample.c, click OK.
7. Right Click the main.c file in the Workspace, select remove.

8. Right Click DevBdExample.c in the Workspace, select “Options”. The following options shown in screen captures will need to be changed.
9. Under General Options, select the tab labeled “Target”. In the Processor configuration pulldown select -cpu=m3000. M3000.

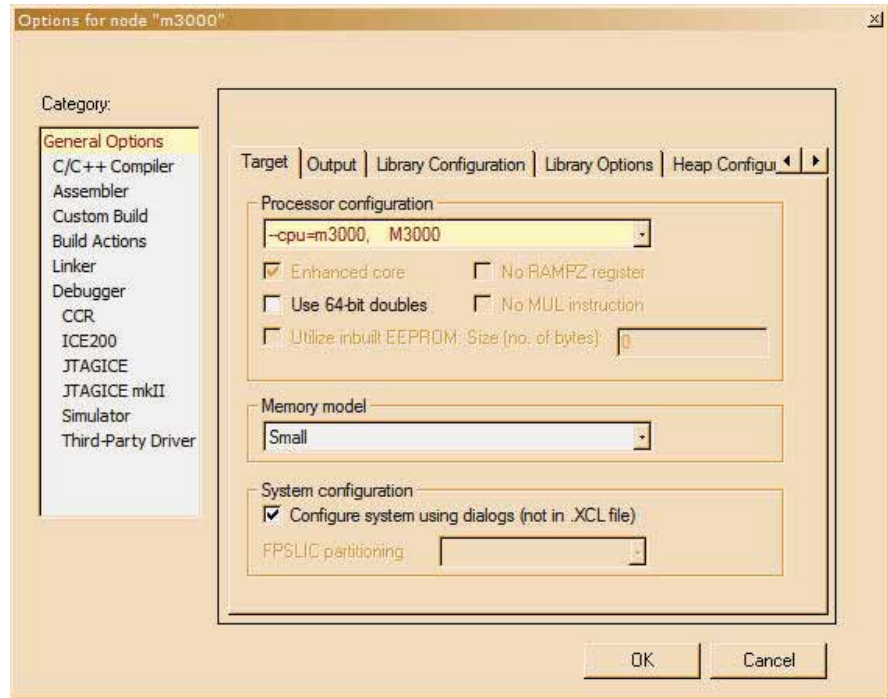


Figure 7.2: Processor Selection

10. Select the General Options tab labeled “System”. Nothing need be changed here at this time, be aware that for larger programs the CSTACK and RSTACK values may need to be increased.

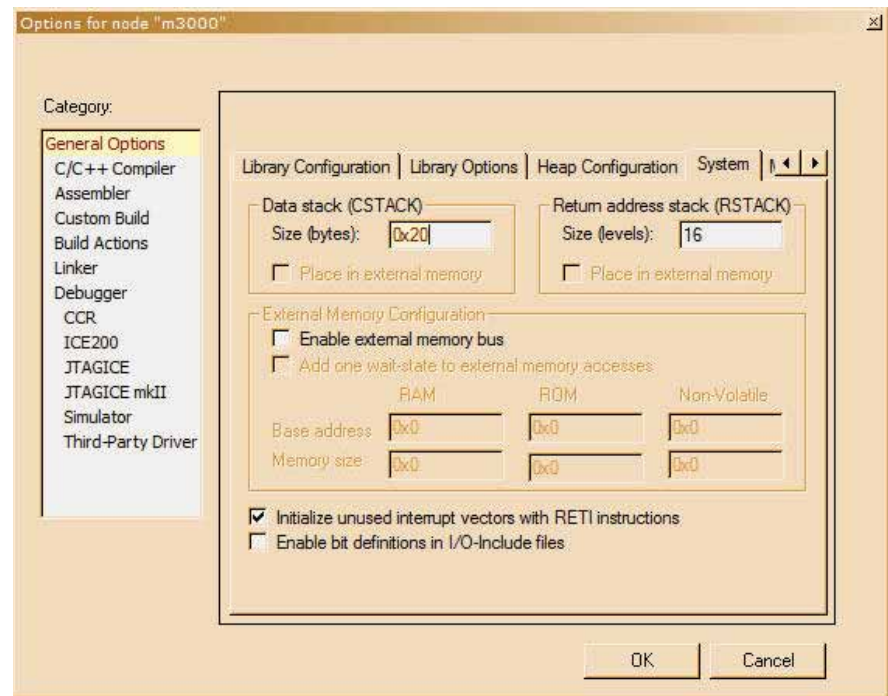


Figure 7.3: Stack Values.

11. Select the Category “Linker”, Select the “Output” tab. Check the check box labeled “Allow C-SPY specific extra output file”

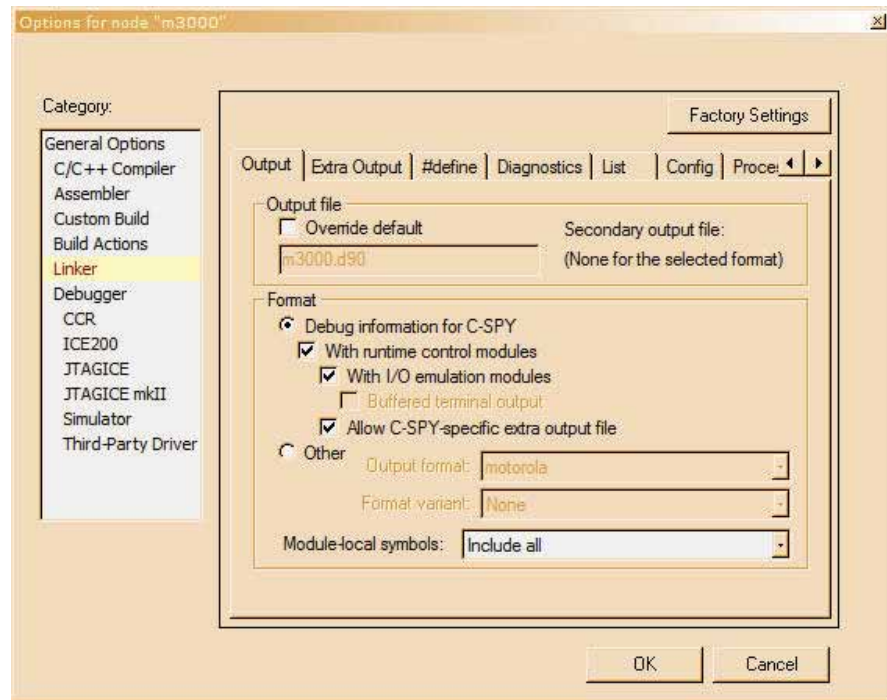


Figure 7.4: Allow C-SPY Extra Output File

12. Select the tab labeled “Extra Output”. Check the “Generate Extra Output File” box. In the Format pulldown, select “intel-extended”.

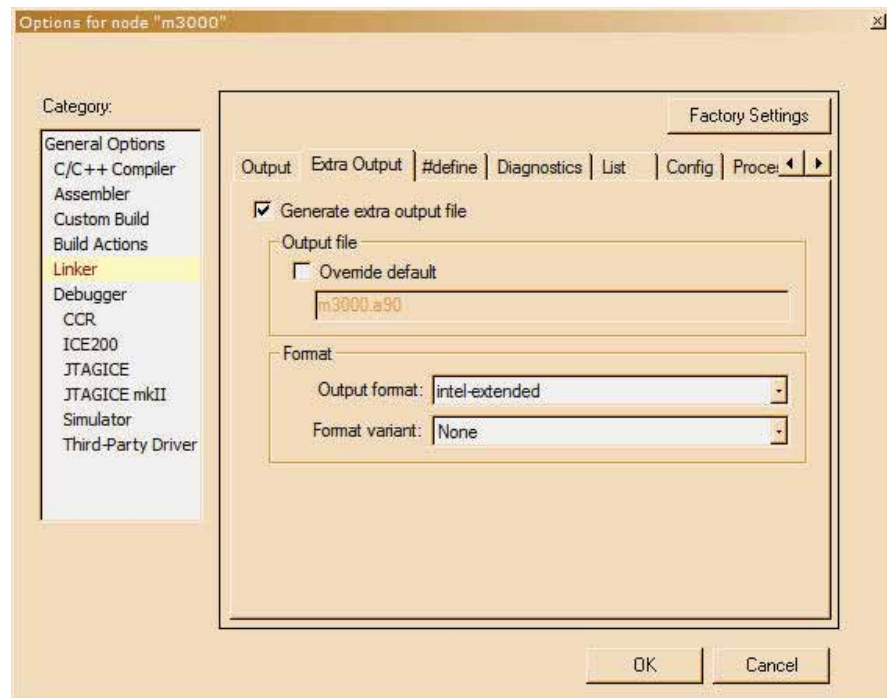


Figure 7.5: Extra output file format

13. Select the category “JTAGICE” On the tab labeled “JTAGICE 1”, Select the COM port your SSI JTAG ICE converter is connected to.

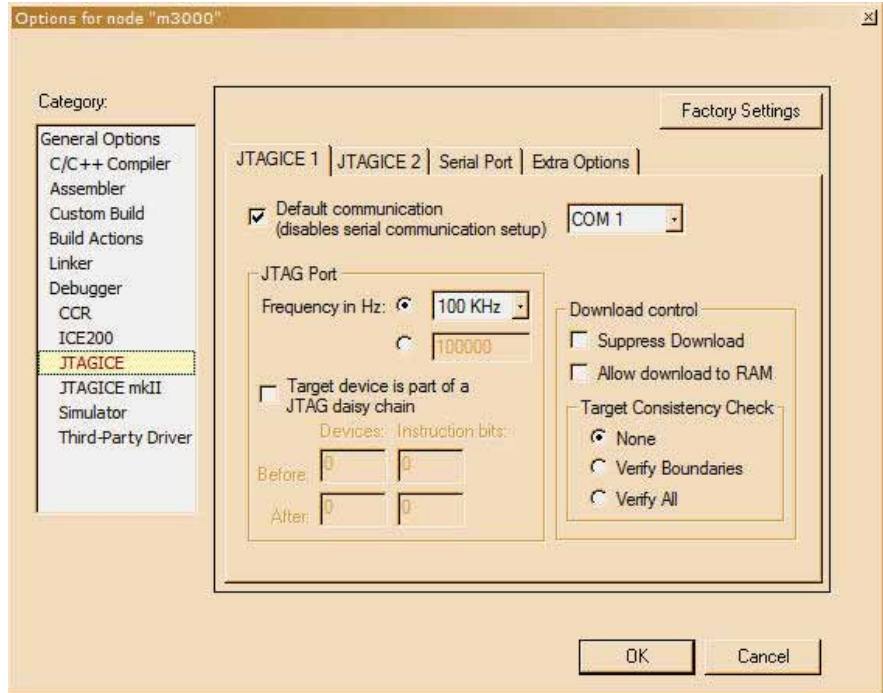


Figure 7.6 JTAG-ICE Setup

WARRANTY

System Semiconductor (“SSI”), warrants only to the purchaser of the Product from SSI (the “Customer”) that the product purchased from SSI (the “Product”) will be free from defects and meets the applicable specifications at the time of sale. Customer’s exclusive remedy under this Limited Warranty shall be the repair or replacement, at Company’s sole option, of the Product, or any part of the Product, determined by SSI to be defective.

This Limited Warranty does not extend to any Product damaged by reason of alteration, accident, abuse, neglect or misuse or improper or inadequate handling; improper or inadequate wiring utilized or installed in connection with the Product; installation, operation or use of the Product not made in strict accordance with the specifications and written instructions provided by SSI; use of the Product for any purpose other than those for which it was designed; ordinary wear and tear; disasters or Acts of God; unauthorized attachments, alterations or modifications to the Product; the misuse or failure of any item or equipment connected to the Product not supplied by SSI; improper maintenance or repair of the Product; or any other reason or event not caused by SSI.

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